



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,063	03/31/2004	William C. DeLeeuw	42339-199426	5261
26694	7590	07/20/2006	EXAMINER	
VENABLE LLP			CHEN, ALAN S	
P.O. BOX 34385			ART UNIT	
WASHINGTON, DC 20045-9998			PAPER NUMBER	
			2182	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/813,063	Applicant(s) DELEEuw, WILLIAM C.	
	Examiner Alan S. Chen	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 18-20 are rejected under 35 U.S.C. 101 because the claims are not limited to tangible embodiments. In view of Applicant's disclosure, paragraph 15, the machine-accessible medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., paragraph 15, ROM, RAM, flash/magnetic storage devices) and intangible embodiments (e.g., paragraph 15, carrier waves and signals). As such, the claim is not limited to statutory subject matter and is therefore non-statutory. To overcome this rejection the claims need to be amended to include only the physical computer media and not include communication/transmission media or other intangible or non-functional media.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 and 9-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Pat. No. 5,768,598 to Marisetty et al. (Marisetty).

5. Per claim 1, Marisetty discloses an apparatus, comprising: a communication device (*Fig. 1, element 103, communicates between I/O devices, elements 104X, and CPU, element 101*) supporting communication using at least two communication protocols (*Column 6, lines 35-40, PGA shown in Fig. 1, element 103 supports multiple external interface protocols; Column 5, lines 60-65 disclose each CLB shown in Fig. 1, element 103X, are configured to a communicate using a particular interface protocol*), wherein said communication device (*Fig. 1, element 103*) is adapted to be coupled to at least two communication interfaces (*Fig. 1, elements 113X are a plurality of interfaces to I/O devices, elements 113X*).

6. Per claim 2, Marisetty discloses claim 1, Marisetty further disclosing said at least two communication interfaces are coupled to a single computing platform (*Fig. 1, element 101, CPU is coupled to I/O devices via PGA, element 103 and respective communications interfaces, element 113X*).

7. Per claim 3, Marisetty discloses claim 1, Marisetty further disclosing said communication device comprises software to configure the communication device (*Column 5, lines 55-67, PROM, Fig. 1, element 105 contains code that is downloaded to configure the PGA, element 103*) to communicate using each of said at least two communication protocols (*Column 5, lines 60-63, the CLB 103A are configured to provide the necessary interface protocol by the code downloaded from PROM, element 105*).

8. Per claim 4, Marisetty discloses claim 1, Marisetty further discloses said communication device comprises a reconfigurable communication system (*Fig. 1,*

element 103, the PGA is by definition a reprogrammable/reconfigurable gate array; once powered off, it will lose fuse connections structure).

9. Per claim 5, Marisetty discloses a system (*all of Fig. 1*) comprising: a communication device (*Fig. 1, element 103*) supporting communications using at least two communication protocols (*Column 6, lines 35-40, PGA shown in Fig. 1, element 103 supports multiple external interface protocols; Column 5, lines 60-65 disclose each CLB shown in Fig. 1, element 103X, are configured to a communicate using a particular interface protocol*); a computing platform (*Fig. 1, element 101 is the processor for computations*); and at least two communication subsystems coupled to said computing platform (*Fig. 1, elements 104X are I/O device subsystems*), each of said communication subsystems adapted to communicate with said communication device using at least one of said at least two communication protocols (*Fig. 1, elements 104X, the I/O devices can communicate with the PGA via two CLBS, that is two possible protocols. Fig. 1, element 103A is a shared protocol, whereas 113X are dedicated protocols*).

10. Per claim 6, Marisetty discloses claim 5, Marisetty further discloses at least a portion of at least one of said communication subsystems is implemented as a device coupled to said computing platform (*Fig. 1, elements 104X are the communication subsystems. These I/O devices are coupled and communicate with the processor, element 101, via the PGA*).

11. Per claim 7, Marisetty discloses claim 6, Marisetty further discloses said device comprises a hardware medium-access device (*Column 5, lines 40-47 disclose I/O*

devices can be a disk controllers or keyboards, both construed to be hardware medium-access devices; Disk controls access hard disks, which is a hardware-medium; Keyboard access computer system, which is construed to be a hardware-medium).

12. Per claims 9 and 10, Marisetty discloses claim 5, Marisetty further discloses communications subsystems (*Fig. 1, element 104X*) is adapted to communicate using more than one communication protocol (*Fig. 1, each I/O devices is shown to communicate over two protocols, one that is a shared protocol, element 112, and one that is a dedicated protocol, element 113*) and changeable between them (*Column 4, lines 43-46, "...a particular I/O device may be both coupled to PGA 103 either using shared and dedicated buses, using only shared bus 112 or using only a dedicated bus..."*; at minimum if the I/O communicating using both shared and dedicated buses, than this meets the condition of "changeable" between two protocols).

13. Per claim 11, Marisetty discloses claim 5, Marisetty further discloses at least one of said communication subsystems comprises: a driver (*Column 6, lines 7 disclose device drivers used in Fig. 1, by CPU/computing platform to operate the IO devices*); and a communications interface coupled to said driver (*Fig. 1, driver controls I/O devices over communication interface lines, element 113X*).

14. Per claims 12 and 13, Marisetty discloses claim 5, Marisetty further discloses said communication device comprises a reconfigurable communication system (*Fig. 1, element 103, the PGA is by definition a reprogrammable/reconfigurable gate array; once powered off, it will lose fuse connections structure*) and is software reconfigurable

(Column 5, lines 55-67, PROM, Fig. 1, element 105 contains code that is downloaded to configure the PGA, element 103).

15. Per claim 14, Marisetty discloses a method, comprising: coupling a communication device *(Fig. 1, element 103, communicates between I/O devices, elements 104X, and CPU, element 101)* to a computing platform *(Fig. 1, element 101, CPU is a computing platform used for computations)*, said coupling comprising: coupling to said computing platform using a first communication protocol *(I/O devices, elements 104X, are coupled to PGA device, element 103 via at least one of two protocols, one dedicated to each I/O device, element 113X, and another that is shared, element 112);* and coupling to said computing platform using a second communication protocol *(Column 1, lines 25-35 describe devices communicating with CPU using distinct protocols; Column 1, lines 52-61 describe shared devices communicating with CPU; Fig. 1 shows I/O devices using these two different types of protocols shared and distinct).*

16. Per claim 15, Marisetty discloses claim 14, Marisetty further discloses said coupling to said computing platform *(Fig. 1, element 101, CPU is computing platform)* using a first communication protocol and coupling to said computing platform using a second communication protocol comprise: sharing a single communication interface coupled to said computing platform *(Fig. 1, I/O devices using different protocols communicate to the PGA, element 103, which in turn interface the CPU, element 101, via a single address/data/control interface, elements 110 and 111).*

17. Per claim 16, Marisetty discloses claim 14, Marisetty further disclosing coupling to said computing platform using a first communication protocol comprises coupling to a first communication interface using said first communication protocol (*Fig. 1, element 103B shows an interface to the PGA using a dedicated I/O device protocol; Element 103B communicates with the CPU, element 101, via PGA, element 103*); and wherein said coupling to said computing platform using a second communication protocol comprises coupling to a second communication interface using said second communication protocol (*Fig. 1, element 103A shows an second interface to the PGA using second shared protocol communicating with the I/O device; Element 103A communicates with the CPU, element 101, using a dedicated I/O device protocol*).

18. Per claim 17, Marisetty discloses claim 14, wherein said coupling a communication device further comprises reconfiguring said communication device (*PGA is reconfigurable*) to communicate utilizing a third communication protocol (*Fig. 1, elements 113X are dedicated communication protocols unique to each I/O devices, thus from Fig. 1 alone, there is shown at least four different communication protocols; Column 1, lines 30-35*), wherein said third communication protocol is used instead of one of said first or second communication protocol (*Fig. 1, element 104B, the I/O device using dedicated protocol 103C, for instance, would clearly use a different protocol than I/O device element 104A as well as different than the shared protocol, element 103A*).

19. Per claim 18, Marisetty discloses a machine-accessible medium (*Fig. 1, element 105*) containing instructions (*Column 5, lines 55-67, PROM, Fig. 1, element 105 contains code that is downloaded to configure the PGA, element 103*) that, when

executed by a processor (*Fig. 1, element 101*), cause said processor to execute a method comprising: configuring said processor to couple, using at least two communication protocols (*Fig. 1, element 113X and 112 are a dedicated protocol and a shared protocol, respectively*), to at least two communication interfaces (*Fig. 1, elements 103B and 103A are two interfaces to I/O device protocols*) coupled to a computing platform (*Fig. 1, element 103, PGA is construed to be the computer platform here*).

20. Per claim 19, Marisetty discloses claim 18, Marisetty discloses containing further instructions (*Fig. 1, element 105*) that, when executed by said processor, cause the method executed by said processor to further comprise: reconfiguring at least one of said at least two communication protocols to a different communication protocol (*Fig. 1, element 103, the PGA is by definition a reprogrammable/reconfigurable gate array; once powered off, it will lose fuse connections structure; Element 105, the PROM reconfigures the PGA to use the shared and/or dedicated protocol; Column 4, lines 43-46, "...a particular I/O device may be both coupled to PGA 103 either using shared and dedicated buses, using only shared bus 112 or using only a dedicated bus..."*).

21. Per claim 20, Marisetty discloses claim 18, Marisetty further discloses said at least two communication protocols comprise at least two different communication Protocols (*Fig. 1, elements 113X and 112, shared and dedicated protocols are different. Shared protocol is usable by all I/O devices, dedicated protocol is device specific*).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. Claim 8 is rejected under 35 USC 103(a) as being unpatentable over Marisetty in view of US Pat. No. 6,654,896 to Saunders et al. (*Saunders*).

Marisetty discloses claim 7.

Marisetty does not disclose expressly the computing platform having a low-power sleep mode where the hardware medium-access device (*e.g.*, *keyboard*) awakens said computing platform from sleep mode upon occurrence of a predetermined event.

Saunders discloses many personal computing systems conserve energy by entering special low power modes, such as sleep modes (*Column 1, lines 12-35*).

Saunders discloses sleep mode being when the clock signal of the computing platform/processors are reduced or halted (*Column 1, lines 45-50*). Saunders further

awakening from sleep mode by activity of the keyboard or hard drive (*Column 1, lines 54-61*).

Marisetty and Saunders are analogous art because they are from the same field of endeavor in computing systems that interface peripheral devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Marisetty to include a sleep-mode and wake upon activity from the keyboard or disk controller as disclosed by Marisetty (*Column 5, lines 40-47*).

The suggestion/motivation for doing so would have been power saving features and powering up only when processing cycles are needed for more efficient use of power that is typical already in many preexisting computer systems (*Column 1, lines 15-20 of Marisetty*).

Therefore, it would have been obvious to combine Marisetty with Saunders for the benefit of efficient power usage.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patents and patent related publications are cited in the Notice of References Cited (Form PTO-892) attached to this action to further show the state of the art with respect to interfacing peripheral devices with a plurality of communication protocols.

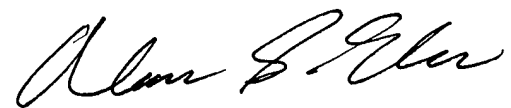
26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

Art Unit: 2182

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC
07/17/2006


2/17/06